Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A data transfer system comprising:

a plurality of first bus devices, at least one first bus device being a first bus data supplying device capable of supplying data, at least one first bus device being a first bus data receiving device capable of receiving data and at least one first bus device being a first bus master device capable of requesting and controlling data transfer;

a first data bus connected to each of said plurality of first bus devices and capable of transferring data from a first bus data supplying device to a first bus data receiving device under control of a first bus master device;

a plurality of second bus devices, at least one second bus device being a second bus data ~~capable of~~ supplying device capable of supplying data, at least one second bus device being a second bus data receiving device capable of receiving data and at least one second bus device being a second bus master device capable of requesting and controlling data transfer;

a second data bus connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device;

a bus bridge connected to said first data bus and said second data bus, said bus bridge capable of supplying data to said first bus, receiving data from said first bus, supplying data to said second bus, receiving data from said second bus,

not capable of controlling data transfer on said first bus and capable of controlling data transfer on said second bus, said bus bridge including

an address first-in-first-out memory having a predetermined number of entries including an input connected to said first bus and an output connected to said second bus, and

a data first-in-first-out memory having said predetermined number of entries including an input connected to said first bus and an output connected to said second bus,

wherein said bus bridge does not allow a read request over the second bus until address first-in-first-out memory and data first-in-first-out memory are empty.

2. (Currently Amended) The data transfer apparatus of claim 1, further comprising:

a first bus arbiter connected to each of said at least one first bus master device and said first bus, said first bus arbiter granting control of data transfer on said first bus to one and only one first bus master; and

a second bus arbiter connected to each of said at least one second bus master device, said second bus and said bus bridge, said second bus arbiter granting control of data transfer on said first bus to one and only one of the set of devices including each second bus master and said bus bridge,

wherein the first data bus is an advanced high performance bus (AHB) and the second data bus is a high performance data transfer bus (HTB).

3. (Original) The data transfer system of claim 1, wherein:

at least one first bus device being a first bus supplying/receiving device capable of both supplying data to said first bus and receiving data from said first bus.

4. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer.

5. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a direct memory access unit which is further capable of controlling data transfer.

6. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a memory which is not capable of controlling data transfer.

7. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer; and

said bus bridge further including at least one control register accessible by said central processing unit, said bus

bridge setting a predetermined buffer full bit of said at least one control register when said address first-in-first-out memory and said data first-in-first-out memory are full.

8. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer; and

said bus bridge further operable to generate an interrupt of said central processing unit when said address first-in-first-out memory and said data first-in-first-out memory are full.

9. (Original) The data transfer system of claim 8, wherein:

said bus bridge further including at least one control register accessible by said central processing unit including a buffer full interrupt enable bit, said bus bridge selectively generating an interrupt of said central processing unit when said address first-in-first-out memory and said data first-in-first-out memory are full and said buffer full interrupt enable bit has a predetermined digital state.

10. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer; and

said bus bridge further including at least one control register accessible by said central processing unit, said bus bridge setting a predetermined buffer empty bit of said at least one control register when said address first-in-first-out memory and said data first-in-first-out memory are empty.

11. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer; and

said bus bridge further operable to generate an interrupt of said central processing unit when said address first-in-first-out memory and said data first-in-first-out memory are empty.

12. (Original) The data transfer system of claim 11, wherein:

said bus bridge further including at least one control register accessible by said central processing unit including a buffer full interrupt enable bit, said bus bridge selectively generating an interrupt of said central processing unit when said address first-in-first-out memory and said data first-in-first-out memory are full and said buffer full interrupt enable bit has a predetermined digital state.

13. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer; and

said bus bridge further including at least one control register accessible by said central processing unit, said bus bridge setting a predetermined buffer full bit of said at least one control register when an entry in said address first-in-first-out memory and said data first-in-first-out memory has been overwritten.

14. (Original) The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer; and

said bus bridge further operable to generate an interrupt of said central processing unit when an entry in said address first-in-first-out memory and said data first-in-first-out memory has been overwritten.

15. (Original) The data transfer system of claim 14, wherein:

said bus bridge further including at least one control register accessible by said central processing unit including a buffer full interrupt enable bit, said bus bridge selectively generating an interrupt of said central processing unit when an entry in said address first-in-first-out memory and said data first-in-first-out memory has been overwritten and said buffer full interrupt enable bit has a predetermined digital state.